WT018684-S5 series Datasheet

Version 1.0.1

July 8, 2022

Wireless-Tag

2.4GHz Wi-Fi(802.11b/g/n) + Bluetooth 5(LE) module

Built around ESP8684 series of SoCs, 32-bit RISC-V single-core processor

Flash up to 4 MB, rich set of peripherals

On-board PCB antenna and external antenna connector

Ordering Code	Chip Embedded	Flash(MB)	PSRAM(MB)	Antenna
WT018684-S5-N1	ESP8684	1	0	PCB
WT018684-S5-N2	ESP8684	2	0	PCB
WT018684-S5-N4	ESP8684	4	0	PCB
WT018684-S5U-N1	ESP8684	1	0	IPEX
WT018684-S5U-N2	ESP8684	2	0	IPEX
WT018684-S5U-N4	ESP8684	4	0	IPEX

About the Document

This document provides users with WT018684-S5 series specification.

Document Version

Please go to the official website of wireless-tag to download the latest version of the document.

Revision History

Please go to the Revision History page to view the revisions.

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Revision History

No.	Version	Changes	Notes	Editor	Date
1	V1.0.0	C	First release	GUO	April 27, 2022
2	V1.0.1	M	Errata, correction 5.1	GUO	July.8,2022

*Changes：C——create，A——add，M——modify，D——delete

Table of Contents

1 Module Overview

1.1 Features

MCU

- ESP8684 SoC embedded, 32-bit RISC-V single-core processor, up to 120 MHz
- 576 KB ROM
- 272 KB SRAM （16KB for cache）
- SIP flash
- Flash controller with cache
- Supports flash in Circuit Programming (ICP)

Wi-Fi

- IEEE 802.11 b/g/n compliant
- Supports 20MHz bandwidth in 2.4GHz band
- 1T1R mode with data rates up to 72.2Mbps
- Data rates up to 72.2 Mbps in 802.11n mode
- Frame aggregation (TX/RX A-MPDU, TX/RX A-MSDU)
- Immediate Block ACK
- Fragmentation and defragmentaion
- Transmit opportunity(TXOP)
- Automatic Beacon monitoring（hardware TSF)
- Wireless multimedia（WMM）
- 3 × virtual Wi-Fi interfaces
- Antenna diversity
- Supports external power amplifier
- Simultaneous support for Infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode

Note that when ESP8684 scans in Station mode, the SoftAP channel will change along with the

Station channel.

Bluetooth

- Bluetooth low energy（Bluetooth LE）:Bluetooth 5
- High power mode
- Speed: 125kbps, 500kbps, 1Mbps, 2Mbps
- Advertising Extensions
- Multiple Advertisement Sets
- Channel Selection Algorithm #2
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

Hardware

- Peripheral interfaces: 14xGPIO, 3xSPI, 2xUART, I2C master, LED PWM controller with up to 6 channels, General DMA controller (GDMA) with 1 receive channel and 1 transmit channel
- Analog interfaces: 1×12-bit SAR ADCs with up to 5 channels, 1x temperature sensor
- Timers: 1x54-bit general-purpose timer, 2x watchdog timers, 1x52-bit system timer

1.2 Description

The WT018684-S5 and WT018684-S5U modules are based on ESP8684, which is a highly integrated and low-power system-on-chip (SoC) supporting Wi-Fi and Bluetooth, designed for Internet of Things (IoT), mobile devices, wearable electronics, smart homes, such as wake word detection, speech recognition, face recognition, smart control panels, smart speakers, etc. The ESP8684 chip features state- of -the -art power and RF performance, complying with the Wi-Fi IEEE802.11b/g/n protocol and BLE 5.0. The chip integrates a 32-bit RISC-V single-core processor, up to 120 MHz. You can

power off the CPU and make use of the low-power co-processor to constantly monitor the peripherals for changes or crossing of thresholds. It supports a secondary development without the need for additional microcontrollers or processors. The chip supports a variety of low-power working states, which can meet the power consumption requirements of various application scenarios. The unique features of the chip, such as fine-grained clock gating, dynamic voltage and frequency scaling, and RF output power adjustment, can achieve the best balance between communication distance, communication rate and power consumption. The WT018684-S5 and WT018684-S5U modules integrate a rich set of peripherals, ranging from UART，SPI，I2S，I2C，ADC，temperature sensor, GPIO, LED PWM controller, GDMA, general-purpose timer, watchdog timer.

The WT018684-S5 and WT018684-S5U modules have a variety of unique hardware security features ensured by the cryptographic hardware accelerators that support AES, SHA and RSA algorithms. RNG, HMAC and digital signature modules provide more security performance. Other security features include flash encryption, secure boot, signature verification. Reliable security features make the SoC perfect for a variety of encryption products. The WT8684-S5 module supports Bluetooth Low Energy: Bluetooth5, Bluetooth mesh. Bluetooth speed supports: 125kbps, 500kbps, 1Mbps, 2Mbps. It aslo supports advertising extensions, multiple advertisement, channel selection. WT018684-S5 and WT018684-S5U are generic Wi-Fi+Bluetooth LE MCU-based modules, integrated with ESP8684 series of SoCs.

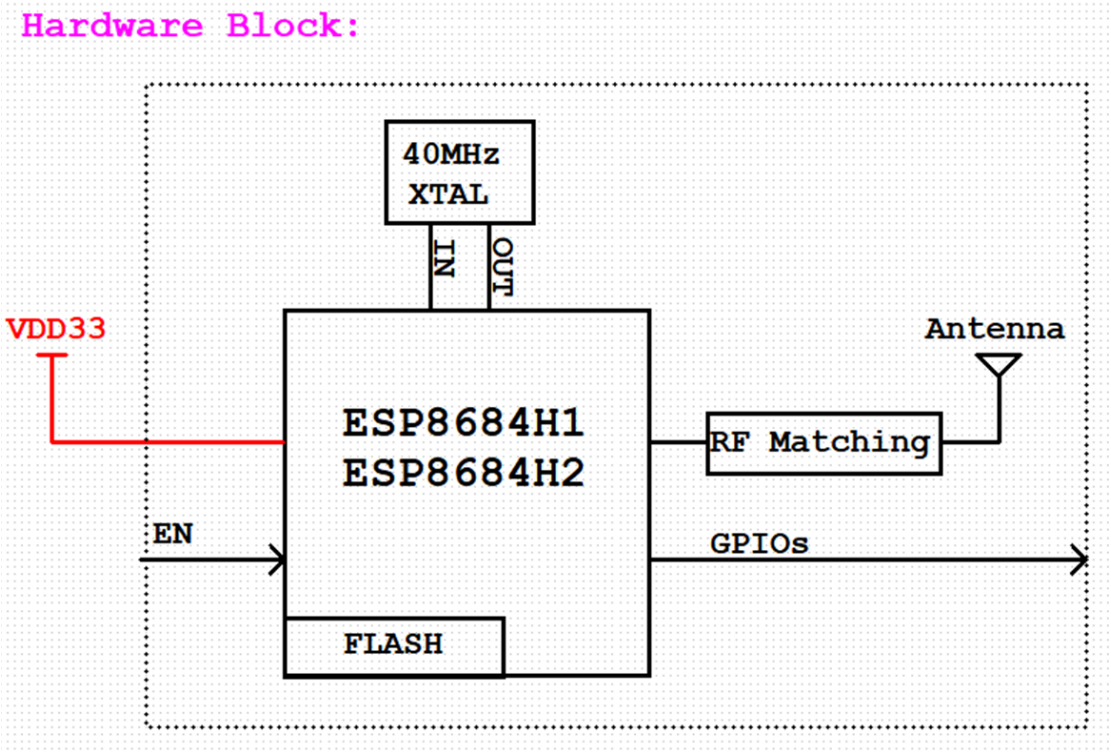
1.3 Applications

- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) devices
- Speech recognition
- Image recognition
- Mesh network
- Home automation
- Smart home control panel
- Smart building

- Industrial automation
- Smart agriculture
- Audio device
- Health/Medical/Nursing
- Wi-Fi enabled toys
- Wearable electronics
- Retail & Catering Applications
- Smart POS machines
- Smart door lock

2 Block Diagram

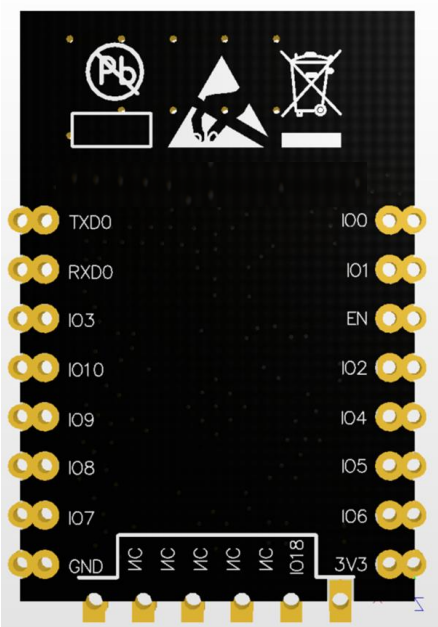
Figure 1 Block Diagram



3 Pin Definitions

3.1 Pin Layout

Figure 2 Pin Layout



3.2 Pin Description

Table 1 Pin Definition and Description

Index	Name	Type	Power Domain	Function
1	IO0	I/O/T	VDD3P3_RTC	GPIO0,ADC1_CHO
2	IO1	I/O/T	VDD3P3_RTC	GPIO0,ADC1_CH1
3	EN	I	VDD3P3_RTC	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the CHIP_EN pin floating.
4	IO2	I/O/T	VDD3P3_RTC	GPIO2,ADC1_CH2，FSPIQ
5	IO4	I/O/T	VDDP3_CPU	GPIO4，ADC1_CH4,FSPIHD,MTMS
6	IO5	I/O/T	VDDP3_CPU	GPIO5,FSPIWP,MTDI
7	IO6	I/O/T	VDDP3_CPU	GPIO6,FSPICLK,MTCK

8	3V3	P_A	-	Analog power supply
9	GND	G	-	Ground,FSPID,MTDP
10	IO7	I/O/T	VDDP3_CPU	GPIO7
11	IO8	I/O/T	VDDP3_CPU	GPIO8
12	IO9	I/O/T	VDDP3_CPU	GPIO9
13	IO10	I/O/T	VDDP3_CPU	GPIO10,FSPICSO
14	IO3	I/O/T	VDDP3_CPU	GPIO3,ADC1_CH3
15	RXDO	I/O/T	VDDP3_CPU	GPIO19,U0RXD
16	TXDO	I/O/T	VDDP3_CPU	GPIO20,U0TXD
17	GPIO18	I/O/T	VDD3P3_CPU	GPIO18
18	NC	I/O/T	-	Dangling pins

P_A: Analog power supply

P_D: Digital IO power supply

I: Input

O: Output

T: High impedance

The pin function in this table refers only to some fixed settings and do not cover all cases for signals that can be input and output through the GPIO matrix.

3.3 Strapping Pins

ESP8684 series has two strapping pins:

- GPIO8
- GPIO9

Software can read the values of GPIO8 and GPIO9 from GPIO_STRAPPING field in GPIO_STRAP_REG register.

During the chip's system reset, the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

There are several types of system resets:

- Power-on reset
- RTC watchdog reset
- Brownout reset
- analog super watchdog reset

By default, GPIO9 is connected to the internal weak pull-up resistor. If GPIO9 is not connected or connected to an external high-impedance circuit, the latched bit value will be "1".

To change the strapping bit values, you can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP8684 series.

After reset, the strapping pins work as normal-function pins.

See Table 2 for detailed booting configurations of the strapping pins

Table 2 Strapping Pins

Booting Mode			
Pin	Default	SPI Boot	Download Boot
GPIO8	N/A	Don't care	1
GPIO9	Internal weak pull-up	1	0
Enabling/Disabling ROM Messages Print During Booting			
Pin	Default	Function	
GPIO8	N/A	When the value of eFuse field EFUSE_UART_PRINT_CONTROL is 0 (default), print is enabled and not controlled by GPIO8. 1, if GPIO8 is 0, print is enabled; if GPIO8 is 1, it is disabled. 2, if GPIO8 is 0, print is disabled; if GPIO8 is 1, it is enabled. 3, print is disabled and not controlled by GPIO8.	

The strapping combination of GPIO8=0 and GPIO9=0 is invalid.

Figure 3 shows the setup and holding times of the strapping pins before and after the CHIP_EN signal goes high. Details about the parameters are listed in Table 3.

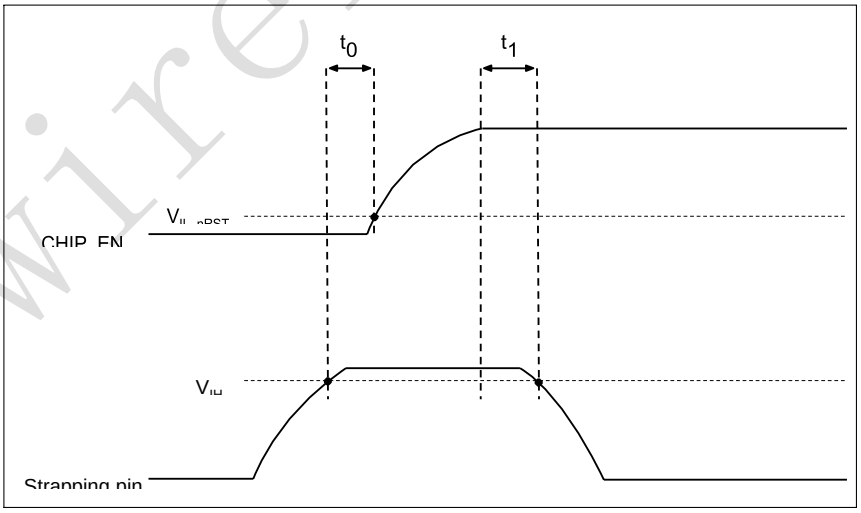


Table 3 Parameter Descriptions of Setup and Hold Times for the Strapping Pins

Parameter	Description	Min（ms）
t_0	Setup time befor CHIP_EN goes from low to high	0
t_1	Hold time after CHIP_EN goes high	3

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses above those listed in *Absolute Maximum Ratings* may result in permanent damage to the device. These are stress ratings only and functional operation of the device is not implied.

Table 4 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDDA3P3, VDDA, VDD3P3_RTC, VDD3P3_CPU	Power pin voltage	-0.3	3.6	V
TSTORE	Storage temperature	-40	150	℃

4.2 Recommended Operating Conditions

Table 5 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDA3P3,VDDA,VDD3P3_RTC,VDD3P3_CPU	Power pin voltage	3.0	3.3	3.6	V
IVDD 2	Current delivered by external power supply	0.5	-	-	A
TA	Operating ambient temperature	-40	-	105	℃

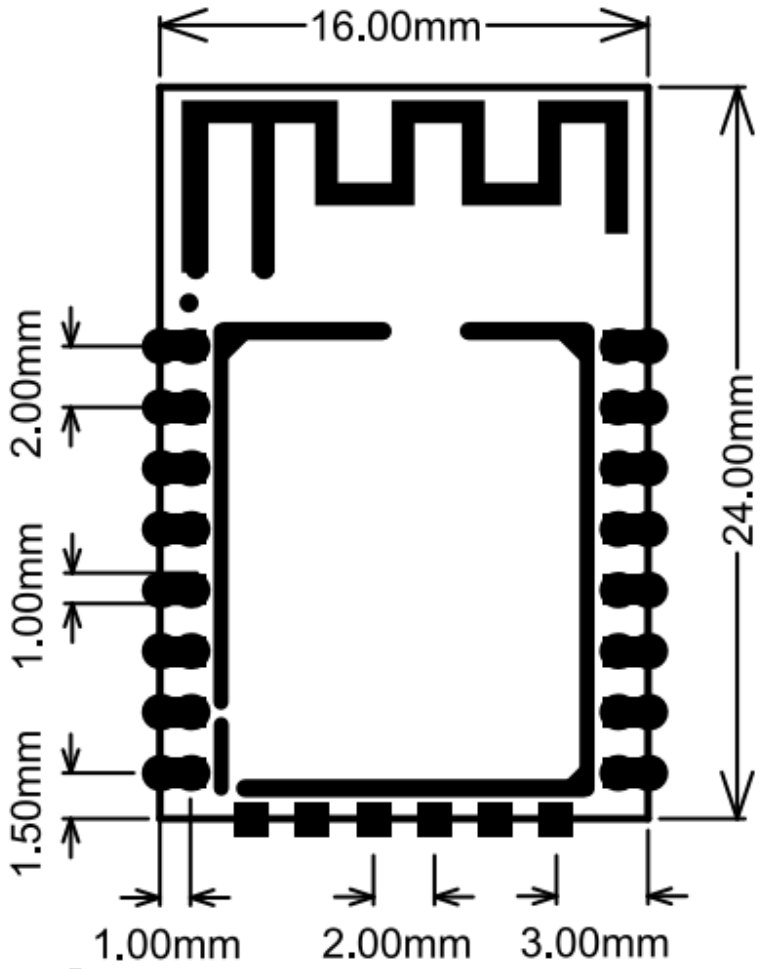
When writing eFuse, VDD3P3_CPU should not exceed 3.3v.

When powered by a single power supply, the output current should reach 500mA and above.

5 Application Notes

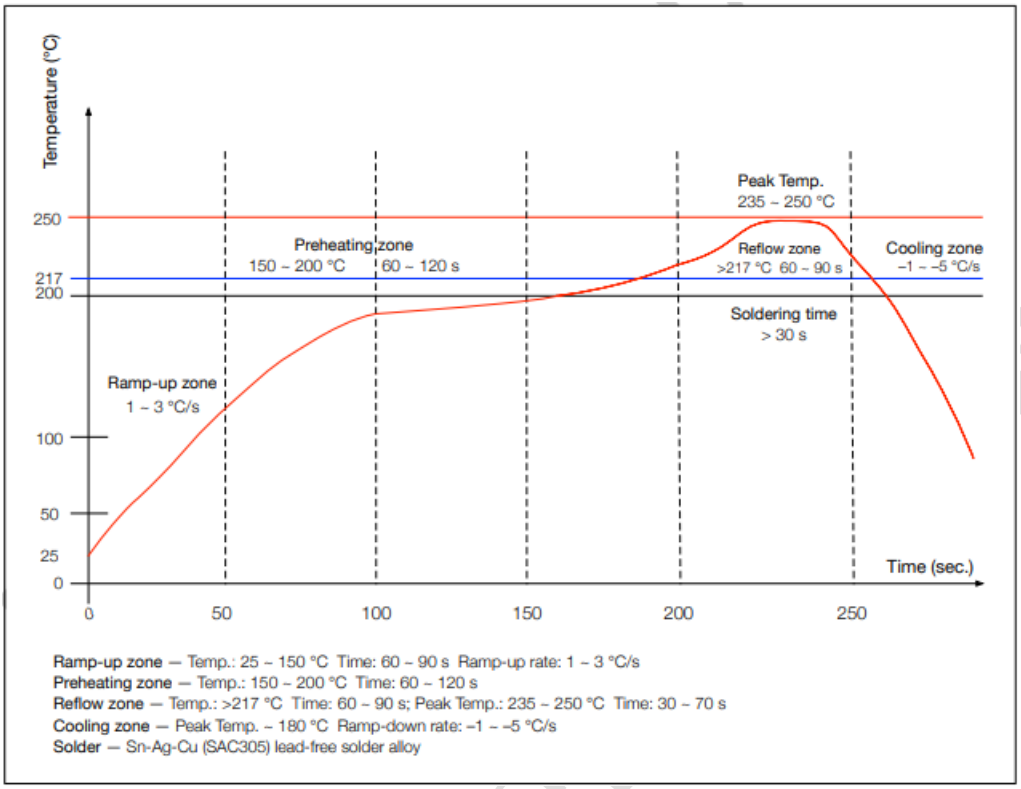
5.1 Module Dimensions

Figure 4 Module Dimensions(Front view)



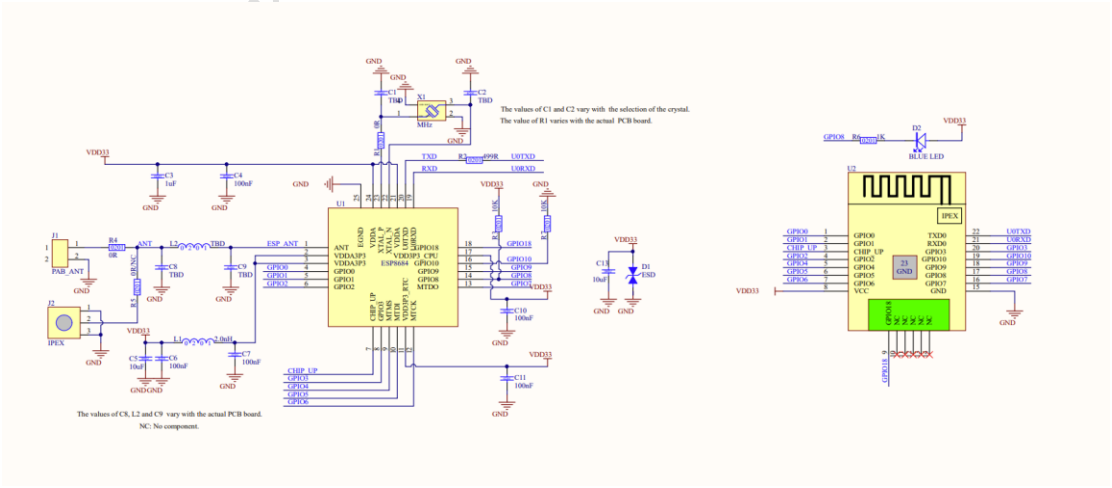
5.2 Reflow Profile

Figure 5 Reflow Profile



5.3 Module Schematics

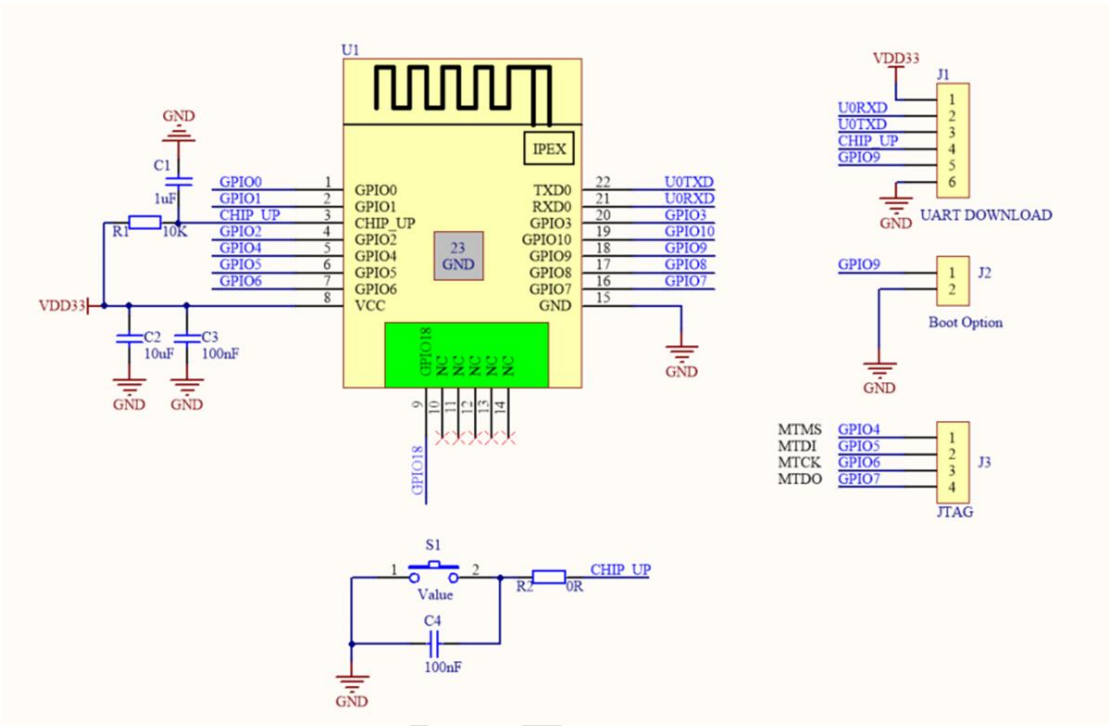
Figure 6 Module Schematics



5.4 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, reset button, JTAG interface, UART interface, etc).

Figure 7 Peripheral Schematics



6 Product Trial

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